

Appl. No. 10/707,700
Amdt. dated April 20, 2005
Reply to Office action of March 23, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (original): A method for writing a memory cell comprising:

5 providing a memory cell comprising an N-type well, three P-type doped regions formed on the N-type well, a first stacked dielectric layer formed on the N-type well and between a first doped region and a second doped region from among the three P-type doped regions, a first gate formed on the first stacked dielectric layer, a second stacked dielectric layer formed on the N-type well and between a second doped region and a third doped region from among the three P-type doped regions, a second gate formed on the second stacked dielectric layer;

10 applying a common voltage to the N-type well, the first doped region and the second gate;

15 applying a voltage less than the common voltage to the first gate in order to erase charges stored in the first stacked dielectric layer;

applying a first voltage to the first gate and a second voltage larger than the first voltage to the second gate, in order to conduct respectively P-type channels between the first doped region and the second doped region and the second doped region and the third doped region;

20 applying a voltage larger than the second voltage to the N-type well and the first doped region; and

25 applying a voltage less than the second voltage to the third doped region in order to inject channel hot hole induced hot electrons into the second stacked dielectric layer formed on the N-type well and between the second doped region and the third doped region.

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2 (original): The method of claim 1 wherein each stacked dielectric layer comprises:
a first silicon dioxide layer formed on the N-type well;
a charge storage layer formed on the first silicon dioxide layer; and
a second silicon dioxide layer formed on the charge storage layer.

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3 (original): The method of claim 2 wherein charge storage layer is composed of silicon nitride (Si_3N_4).

4 (original): The method of claim 2 wherein charge storage layer is composed of silicon
10 oxynitride ($Si_xN_yO_z$).

5-14 (cancelled).